Date: Sat, 27 Jul 2002 08:16:42 -0700
From: Scott Bernardi
Subject: Re: VC RADSR help please

I made some mods to the vcradsr to make it re-triggerable. I also added a
level pot and some gain on the output so you can vary the output peak from
0 to 10v. I just uploaded the schematic to the EFM_Synth Files section.
The schematic is completely redrawn, so the parts numbers are all
different, but look on the left near the GATE and TRIGGER inputs and
compare it to Tom's original circuit. Trigger levels depend on what you
run the supply voltages at for the digital IC's - the threshold is at 1/2
the supply voltage. If you want to standardize on say 5v trigger levels,
you can add a couple oftransistor inverters (like Q3 on my circuit). Come
to think of it, I'll probably do that on my circuit in front of the
Trigger input. When I breadboarded the circuit, I got delay times from
less than a millisecond to several minutes. Note that I have reduced the
charging cap from .05uF to .01uF. I also changed (R12 on Tom's circuit,
R13 on mine) from 1K to 2.2K

Date: Sun, 28 Jul 2002 04:52:53 -0500
From: "e4m"
Subject: Re: VC RADSR help please

Nice mods Scott....but you make it sound like the stock board is not re-
triggerable and it's a function you added. The vcradsr was designed from
the very start to be re-triggerable and the option is on the board.

Tom

Date: Sun, 28 Jul 2002 21:00:16 -0700
From: Scott Bernardi
Subject: Re: VC RADSR help please

Guess I missed that because the schematic doesn't have separate Gate and
Trigger inputs. I guess that's what the "Trigger/Gate" switch is for.
Correct me if I'm wrong - what I'm thinking of as "retrigerrable" is when
you have a note held down, then press another key. The Gate stays high,
but if you have a separate Trigger that pulses whenever a key is pressed,
you can retrigger the Attack-Decay portion of the envelope. As far as I
know, that requires a separate Gate and Trigger input. How does the vc-
radsr work? By the way Tom, excellent design. I also looked at Juergen
Haible's VC ADSR, but yours seemed much simpler.

Date: Mon, 29 Jul 2002 03:54:10 -0500
From: "e4m"
Subject: Re: VC RADSR help please

Ahhh I see it's a term thing...I call it retriggered when the the level
falls to almost zero and the eg re-triggers itself. As in the LFO mode.
What you're talking about I would call keyed and that's built into the
logic function. When the gate is removed the 4052 switches to release mode
regardless of where it is in it's cycle. If the gate is reapplied it

starts it's cycle again immediately. Again regardless of where it's at. In effect it's restarted before it reaches zero. In triggered mode the eg will complete it's cycle ignoring all incoming control messages to do otherwise and will not trigger again until done. Unless you have a way to set sustain time in addition to level an adsr can't function in triggered or lfo mode. So the vc radsr also switches to vc-rar when switched to a trigger input and the trigger/gate switch should be set to trigger when LFO mode is engaged. If not it can hang up when it gets to the sustain part of the cycle.
I have a triggered adsr with variable sustain time it works really well and I might release it someday but it's not really that useful in the big scheme of synth things.
Juergen is a bonafide genius. He reverse engineered the Curtis gm cell and used the core to design his vc adsr. It has all sorts of advantages and very few gotchas. It's true it's more complicated and less functional but like Juergen it's very special. Once you get the hang of the cell it's possible to build just about anything you want with it....
I can say no more...

Tom

Message: 4
Date: Mon, 29 Jul 2002 10:51:21 -0700
From: "Fahl, Romeo"
Subject: RE: VC RADSR help please

I have a (possibly dumb) question about the EFM VCADSR:

Is there any harm in putting negative voltages into the VC inputs? Since the 4052 is running of +V and Ground, I thought that it could freak it out if you try pushing a negative voltage through it.

Date: Mon, 29 Jul 2002 14:10:11 -0500
From: "e4m"
Subject: Re: VC RADSR help please

The short answer is no....a slightly longer answer is that there isn't enough current there to do any real harm but there's no real point ether. It's not a stock option but you can run the 4052 on +5/-12 The logic will still work and it can handle +/-5Vpp at it's inputs. If you need a wider range swap a pair of DG212s for the 4052. Of course the values of everything else in the circuit will have to be changed too. As is, it expects a positive voltage.

Tom

Date: Sat, 14 Sep 2002 10:55:47 -0400
From: Dave Magnuson
Subject: ADSR mod from SDIY

      Hi List,

      I just got a post from SDIY that I thought some of you might enjoy. Peter
      Grenader sent a link to his modification to an analog solution's ADSR to
      add an end-of-cycle pulse output
      This mod could be applied to any ADSR that will retrigger (LFO mode) like
      the VC-R-ADSR. All it does is buffer the reset pulse with a simple
      transistor circuit and bring it out to a jack. He mentions using the ADSR
      as a gate delay, or chaining 2 ADSRs sequentially to get more complex
      envelopes.
      To hook it to a VC-R-ADSR, you'd simply attach his circuit to the reset
      line that connects to the LFO/EG switch (the trace from pin 14 of U4 to
      S2).
      I hope to add this feature to one of my VC-R-ADSR's, and I'll let you all
      know how it goes! I currently don't have a gate delay, and this is such a
      simple way to achieve it (I have 4 VC-R-ADSR, so I can "sacrifice" one and
      use it as a delay when needed)

Posted 09/17/2005 10:18:18 PM

      Unlike my post regarding VCF12a mods, these mods actually make the VC
      RADSR behave much more predictably and also make it much more usable.
      Put the clock buffer subcircuit from Ken Stone's Gated Comparator before
      the "Gate" input on the VC RADSR
      Don't use an LM358 as the opamp in the clock buffer circuit, use a TL072
      (some 358s are too slow and you don't know until you put it in the
      circuit, save yourself the pain). With this installed, the VC RADSR
      triggers/gates much more reliably. Before, if it wasn't receiving a very
      stiff clock pulse, it wouldn't trigger. And often the gate mode didn't
      work at all. Now it works fine.
      I also modded it to make the output envelope +10V instead of +5v. Here's
      how:
      1. Wire jumper from "Out" on PCB to Pad 1 on "Offset In"
      2. Leave R29 & R30 installed as they are on the schematic (any 2 matching
      values will do)
      3. Wire jumper Pad 2 to Pad 3 on "Offset In"
      This sets up the offset op amp in U4 to be a non-inverting amplifier with
      a gain of 2. The new ADSR Out comes from the "Offset Off" pad on the PCB.
      I attached this to an attenuating Level pot, so I can adjust the value
      down as need be.
      Please note that this text refers to the labeling on the PCB, which has a
      mistake on it when compared to the schematic. If you're making this mod
      based on the schematic, you would just switch Pad 2 and Pad 1 in the
      procedure above.
      Another mod I did was to add an "End of Cycle" pulse output. Basically a
      pulse is generated internally when the VC RADSR is ending its cycle. This
      signal is what is used to retrigger the VC RADSR when in LFO mode. It
      appears at pin 14 of U4. Buffer this output - I used another Ken Stone
      subcircuit, the transistor buffer from many of his designs, for example
      the Burst Generator.This output lets me chain together the VC RADSR with
      other ADSRs to make longer complex envelopes, as well as using it to clock
      many other cool timing events.
      Enjoy...
      -Chris

xamboldt
Posted 09/18/2005 6:48:03 PM

I realized something after I typed this - instead of using the transistor
buffer for the end of cycle out, you could just use the unused half of the
TL072 left over from the gate buffer....
-Chris

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xamboldt
Posted 10/21/2005 03:06:25 AM

Even more mods!
After I posted these previous mods, Dave Kendall provided me with some
details of further mods that Scott Bernardi had posted to the old yahoo
group. Dave and I bounced around some ideas and I just got around to
trying them out. The basic idea is to make the EG retrigger if a new
trigger signal is received before the original ADSR cycle is complete (ie
before the gate is released).
A little background: Some MIDI-to-CV modules send a new trigger pulse for
every new key press, even if a previously struck key is still being held
down. This is a great feature that helps to clean up sloppy keyboard
playing. Now, thanks to the Bernardi mods, my VCRADRS does this.
Basically, you have to isolate the trigger and gate signals within the
VCRADSR.
I removed the Gate/Trigger switch, and used this hole for my new Trigger
In jack. I recommend buffering this signal in the same way I buffered the
Gate Input (see my previously posted mod) - I used the other half of the
TL072 that I had used in my earlier mod. The Trigger In jack after it's
buffered, goes to the "Gate In" hole on the board (which connect to C3).
The Gate In jack, after it's buffered, goes to an outside lug of a DPDT
switch (I re-used my Gate/Trigger switch). In fact, you only have to
disconnect the wires on the Gate Trigger switch that affect the "Sustain"
function, and the wire that connects the "Gate In" pad (where I connected
the "Trigger In" signal) to the switch.
Then remove the old ADSR/LFO switch, disconnect the wires from the switch
(but not the board), and attach those wires to the DPDT switch, which will
become the New ADSR/LFO switch. Basically, in LFO mode is the same, except
the second pole of the switch is switching the Gate Input high, so that
the LFO will function (it doesn't really work with a low gate). To
clarify, in LFO mode, one pole of the DPDT switch connects +V to the pad
on the board that connects to R16. In ADSR mode, that pad is connected to
the buffered signal from the "Gate In" jack.
The only thing left to do is normal the Trigger In jack to the Gate In
jack, so that if no cable is plugged in to the Trigger In jack, that the
signal at the Gate In jack will go to the Trigger In jack.
Now, if you have only a gate coming in, the VCRADSR operates as it did
before. Buf if you have a gate and a trigger, it will retrigger even if
the original ADSR cycle has not completed. If you want to have a trigger-
only mode, then normal the Gate In jack to +V. Now if you have no cable
plugged in to the Gate In jack, but send a trigger to the Trigger In jack,
you'll get an AD envelope.
One side effect of this mod is that the Sustain control will work all the
time (unless you have something plugged in to the Gate In jack that is
low). This is actually kind of cool, as the Sustain can then be used as
sort of a bias CV for other modules if you're not using the EG. You'll
just have to remember to turn it down if you want a trigger only mode. :)
Also bear in mind that the Sustain works in LFO mode - if it's set past a
certain point, the LFO stops oscillating and the output rests at the

Sustain level. This could also be considered a feature - if you are modulating the Sustain CV with a Square wave, for example, then the LFO output could be "frozen" at the sustain level for the length of the modulating square wave. Or if a different modulating waveform was used, it could be sort of a mini-"psycho" LFO, with the modulating waveform overriding the internal waveform when it surpasses a certain point, and the internal waveform plugging along when the modulating waveform is below that point.
I also tried another mod, but it doesn't add much functionality, and it requires some trace cutting. All it ends up doing is giving you a different kind of Trigger Only mode, where you get an AR envelope instead of an AD envelope. The big difference is that this AR envelope can be triggered even if the gate is low, and the decay and sustain stages are bypassed. I'm not sure yet if this is a bug or a feature. :) If people are interested, I can post details. I'll need to play with it a bit to see even if I want to keep it - I could very well switch it back to the way I mentioned above.
Anyway, good luck! Also, I feel I must say that I am definitely not an electrical engineer - all I do is hack circuits. Sometimes they work, sometimes they don't. This mod happened to work for me. I'm not encouraging you to make these modifications, but just sharing my experience. Please realize that there's always a risk to modding your modules, and I can't be held responsible for any damage to you or your module if something goes wrong.
Sorry for the rambling nature of this post - let me know if anything needs clarification...
-Chris